ABSTRACT

A flash EPROM array (**100**) and method of manufacture is disclosed. Source regions (**118**a-**118**f) are shared between the memory cells (**108**a,l-**108**d,n) of row (**104**a-**104**d) pairs, and are isolated from one another in the row direction by isolation regions **120**. Low resistance source conductor members (**122**a-**122**b) extend in the row direction and are formed over the source regions (**118**a-**118**f) and make contact therewith in a self-aligned fashion. The architecture allows for source decoding and thus enables user programmable sector erase architecture.